Special Lecture in Green Nanotechnology

Nov. 6, 13:00-16:10
Place:機械知能系講義室3

「Research on Post-Si devices based on Ge and 2D channel materials and TCAD Simulation」

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Abstract

The scaling limit of current CMOS technologies has been approaching rapidly. To further enhance performance of CMOS devices, advanced materials such as Ge and 2D materials are promising candidates. We (Advanced Materials and Devices Integration Group in AIST) explore device integration technologies for going beyond the performance limit of Si CMOS. The research topics include Si FinFET, Ge/III-V MOSFETs, 3D build-up integration, 2D channel materials, and devices incorporating new materials and mechanisms such as spin FET and negative capacitance FET. We also focus on methodology and modeling of TCAD simulation and their application for various semiconductor devices. In this talk, I will briefly introduce our current research activities.

Recently, high-performance and low-power LSI is realized by miniaturization and scaling. However, as technology node approaches below 10 nm in 2020s, the end of the scaling is speculated [1]. We are working on 3D build-up integration by vertical stacking of 2D circuits after the end of the scaling [2]. For the stacking channel materials, we are focusing on both Ge and 2D-dichalcogenide materials.

Ge substrate is one of the promising platforms for high-mobility channel transistors and photonic devices. We focus on high-quality Ge platform by bonding epitaxially grown Ge layers to any substrates [3].

Also, 2D-dichalcogenide materials attract much attention because of their unique characteristics. We focus on gas-source CVD of 2D-dichalcogenide and its 3D-stacked device application to realize beyond-Si high-performance and low-power integrated

circuits [4].

In addition, the technology CAD (TCAD), a computer simulation for semiconductor manufacturing process and semiconductor device physics, is very important for the post Si devices. We focus on methodology and modeling of TCAD simulation and their application for various semiconductor devices [5]. We collaborate with other institutes in AIST to apply TCAD simulation for various devices and various projects and we also focus on industrial collaboration.

(Reference)

1. International Roadmap for Devices and Systems (IRDS), 2017 Edition.
2. T. Irisawa et al. VLSI Technology Symposium, 2014.
3. W. H. Chang et al., VLSI Technology Symposium, 2017.
4. T. Irisawa et al., Electron Devices Technology and Manufacturing (EDTM) Conference 2018.
5. https://unit.aist.go.jp/neri/en/ImpulseTCAD/index.html.